Applications and Design of Plated & Filled Via Circuits

Introduction

The introduction of Vishay EFI's Gold or Copper filled vias has solved all of the problems of plated through holes and brought new flexibility to the circuit designer. The task of providing a low inductance, microwave grounding path is handled exceedingly well by filled vias, allowing high performance silicon and gallium-arsenide RF circuits to be assembled in a surface mount configuration.

Assembly concerns are also addressed by eliminating epoxy and solder bleed onto the component mounting surfaces. Furthermore, fewer individual substrates can be used to implement a design by eliminating the need to mount active die to the package floor. Filled vias also act as thermal vias for temperature-critical applications or may be used for two-sided signal interconnection with one of Vishay EFI's multi-layer products.

Circuit designers constrained to the use of plated holes because of ongoing programs or designs which are under configuration control can still benefit from Vishay EFI's mature plated-via process. Years of thin film process experience at Vishay EFI ensures that the engineer will have reliable plated vias for any hi-rel application.

Designing with Plated and Filled Vias

The thin film circuit design process normally begins with the engineer choosing a substrate material and thickness, followed by a via diameter. Subsequent steps include optimization of via placement for high frequency designs followed by a thermal analysis where necessary.

Step 1: Choosing a Via Diameter

Most circuit designers quickly discover that a hybrid circuit design usually benefits from embedded ground connections formed with via holes through the substrate material. These connections provide a convenient means of obtaining a ground return through the case of the mounting medium without the use of cumbersome bond ribbons. Vishay EFI Technology's filled vias provide this interconnection utilizing solid gold or copper metallurgy deposited to the base substrate using proprietary techniques. Careful optimization of the via process has resulted in specific via geometries as a function of substrate thickness.

The first step in the design process, therefore, is to choose the proper via size based upon the desired substrate material. Vishay EFI Technology offers its via-fill process for Polished and Asfired, 99.6 % alumina, aluminum nitride, and beryllium oxide substrates. Available via sizes are shown in Table 1 with dimensional requirements detailed in Figure 1. Designs requiring plated vias enjoy a higher level of diameter and substrate material flexibility as detailed in Table 2. While the minimum via sizes are limited to the listed values for purposes of high yield manufacturing, the maximum via size may be larger than those shown in the table as long as the design is reviewed by your Vishay EFI Technology Sales Engineer.

Table 1 - Filled Via Size as a Function of Substrate Thickness

Substrate Thickness inches (mm)	Minimum Filled Via Diameter inches (mm)[1)]	Filled Via Material	Substrate Material	Via Spacing[2)] Center to Center inches (mm)	Via Spacing[3)] Center to Circuit Edge inches (mm)
0.010 (0.250)	0.006 (0.15)	Au, Cu	Al_2O_3, BeO, ALN	0.012 (0.30)	0.009 (0.23)
0.015 (0.375)	0.008 (0.20)	Au, Cu	Al_2O_3, BeO, ALN	0.016 (0.41)	0.012 (0.30)
0.020 (0.500)	0.010 (0.25)	Au, Cu	Al_2O_3, BeO, ALN	0.020 (0.51)	0.015 (0.38)
0.025 (0.625)	0.012 (0.30)	Au, Cu	Al_2O_3, BeO, ALN	0.025 (0.63)	0.018 (0.46)

Notes
1. Minimum via diameter equals 0.5:1 aspect ratio with absolute minimum at 0.006
2. 2 x via diameter minimum
3. 1.5 x via diameter minimum

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Table 2 - Plated Via Size as a Function of Substrate Thickness

Substrate Thickness inches (mm)	Plated Via Diameter inches (mm)	Plated Via Material	Substrate Material	Via Spacing Center to Center inches (mm)	Via Spacing Center to Circuit Edge inches (mm)
0.005 (0.125)	0.007 - 0.02 (0.175 - 0.50)	Per Metals Guide	Al_2O_3, QTZ	diam. + 0.02, 0.03 min (diam./2 + 0.5)	diam./2 + 0.02 (diam./2 + 0.5)
0.010 (0.250)	0.007 - 0.04 (0.175 - 1.00)	Per Metals Guide	Al_2O_3, BeO, QTZ, AIN, Titanates, Ferrites	diam. + 0.02, 0.03 min (diam./2 + 0.5)	diam./2 + 0.02 (diam./2 + 0.5)
0.015 (0.375)	0.009 - 0.10 (0.225 - 2.50)	Per Metals Guide	Al_2O_3, BeO, QTZ, AIN, Titanates, Ferrites	diam. + 0.02, 0.03 min (diam./2 + 0.5)	diam./2 + 0.02 (diam./2 + 0.5)
0.020 (0.500)	0.012 - 0.10 (0.300 - 2.50)	Per Metals Guide	Al_2O_3, BeO, QTZ, AIN, Titanates, Ferrites	diam. + 0.02 (diam./2 + 0.5)	diam./2 + 0.02 (diam./2 + 0.5)
0.025 (0.625)	0.015 - 0.15 (0.375 - 3.75)	Per Metals Guide	Al_2O_3, BeO, QTZ, AIN, Titanates, Ferrites	diam. + 0.02 (diam./2 + 0.5)	diam./2 + 0.02 (diam./2 + 0.5)

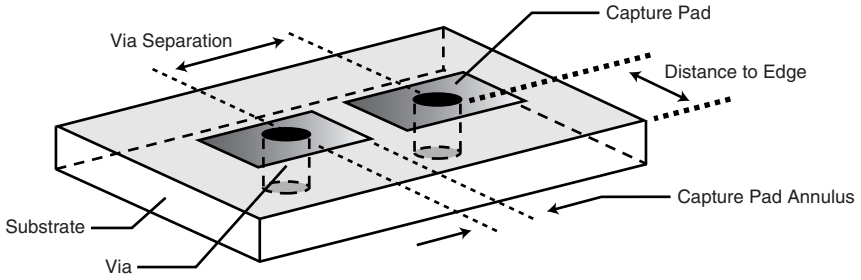

Fig. 1: Dimensional Cinsiderations for Filled Vias

Step 2: Via Modeling and Placement

In higher frequency circuits the designer may also require ground vias, but is concerned with their parasitic effects on circuit performance. From an electrical standpoint, a via hole can be viewed as a series RL circuit with the resistance and inductance values being a function of via metallurgy and geometry. Measurements of the above via structures yields data useful for circuit simulations. These compiled values are shown in Table 3.

A sample comparison of filled via performance versus that of the traditional plated through hole shows an improvement at RF and microwave frequencies due to reduced parasitic resistance. Via inductance values change only slightly due to the similar magnetic field patterns around the metallized cylinder forming the via. Table 4 highlights the reduction in resistance and inductance when filled vias are incorporated into a circuit design. Insertion loss data for a shunt via embedded in a 50 ohm line is compared for filled and plated-via-cases is shown in Figure 2.

In addition to providing interconnect between sides of a substrate, Vishay EFI Technology's unique filled via structure provides a planar surface with low parasitic inductance and resistance for surface-mounting active silicon and gallium arsenide devices. Microwave designers worldwide have reduced ground discontinuity problems by surface mounting MMIC die on a matrix of Vishay EFI Technology's filled vias.

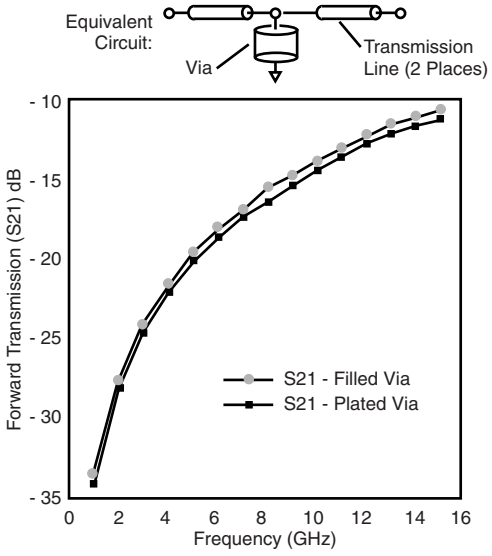

Fig. 2: Shunt Via Transmission (S21)

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Table 3 - Modeling Parameters for Filled Vias

Via Height	Via Diameter	Via Resistance	Via Inductance
0.010"	0.014"	< 0.08 mΩ	20 pH
0.015"	0.014"	< 0.11 mΩ	42 pH
0.020"	0.016"	< 0.11 mΩ	64 pH
0.025"	0.020"	< 0.10 mΩ	78 pH

Table 4 - Filled Via Comparison

Via Type	Via Height	Via Diameter	RC Resistance	RF Resistance at 10 GHz	Inductance
Filled	0.025"	0.020"	0.01 mΩ	4 mΩ	78 pH
Plated	0.025"	0.020"	4 mΩ	14 mΩ	81 pH

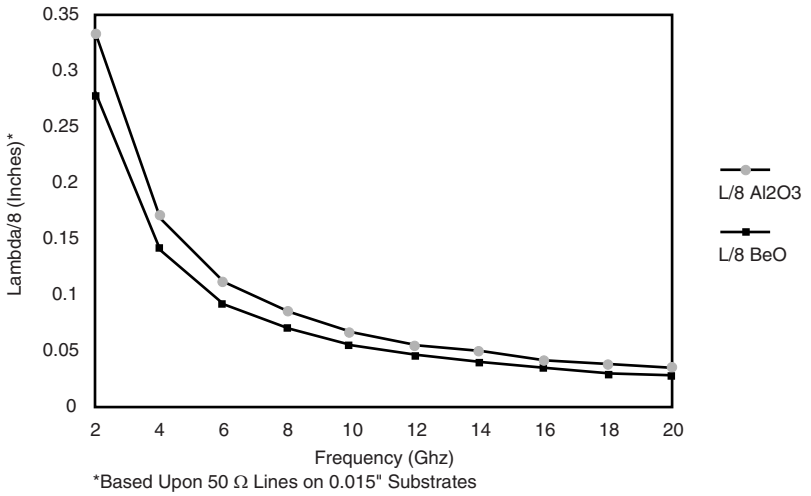
Two approaches for via placement have been used to apply this technology with confidence. Prior to the advent of user-friendly, effective 3-dimensional electromagnetic simulators, a conservative design approach placed vias a maximum of one eighth of a wavelength, center-to-center distance apart in all directions within a chip mounting pad to ensure modefree operation. Wavelength calculations should include the effects of the substrate dielectric constant, effectively reducing the wavelength in air by the square root of the dielectric constant.

The graph shown in Figure 3 provides eighth-wavelength data for 50 Ω transmission lines on 99.6 % alumina and beryllia and may be used as a general guide for via placement. Via spacing must, however, conform to the design rules of Table 1.

Additionally, the designer should opt for a filled via directly under each of the device's RF connections, if possible. This approach, as shown in Figure 4, provides a minimum path length for RF ground current, resulting in improved VSWR.

Advances in finite-element electromagnetic simulators have enabled today's designer to optimize via locations, potentially using fewer vias to obtain comparable performance. By identifying poorly grounded "hot spots" on the ground plane, vias can be used to short circuit these high electric field areas to ground. This analysis approach is beyond the scope of this application note but is covered in a number of published papers.

The limitations of plated holes are particularly apparent in this portion of the circuit design, requiring that all active devices or components be located adjacent to the via hole, rather than over it. In rare cases it is possible to mount an active die over a plated via, provided that the substrate attachment method has been well controlled and that the wire bond sites are located away from the open via holes.



*Based Upon 50 Ω Lines on 0.015" Substrates

Fig. 3: Eighth-Wavelength vs Frequency - Alumina & Beryllia

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Step 3: Review Layout Issues

When laying out a circuit, the design engineer must obey the via hole placement rules identified in this guide and, additionally, must enclose vias with a circular or square metallized capture pad. For filled vias the capture pad must be at least 0.0025" larger, minimum, per side than the via diameter. As an example, 14 mil diameter vias must be located within a minimum 20 mil diameter circular pad or a 20 by 20 mil square pad. A plated hole similarly requires a capture pad, but in this case the pad must be larger than the vias by 0.005" per side, minimum.

As a general rule all filled vias need to be designed with a vented metal structure over the via area - see Fig. 5. This may be placed on front but more commonly is placed on the rear of the substrate. This mitigates the risk of forming blisters around the filled via.

In designs requiring fine line definition plate-up processing, a via venting pattern is required over all filled via metallization. This vent artwork has no impact on the electrical performance of the via and can be applied by Vishay EFI's CAD group prior to mask generation. Circuits will appear similar to those shown in Figure 5. Consult with your Vishay EFI Sales Engineer regarding the need for this technology in your application.

Step 4: Addressing Thermal and Assembly Issues

EFI Technology's unique all-gold or copper via metallurgy provides a high thermal conductivity path through the substrate material to relieve selfheating problems in high-power devices dissipating several watts. Applications such as high power limiter diodes, laser diodes, and Silicon or GaAs amplifiers benefit directly from this surface-mounting approach shown in Figure 4. Previously, electrical designers were limited to mounting high power devices to their respective package or carrier floors to ensure optimal junction temperatures. This approach inevitably required a substrate with a laser-cut opening, or multiple substrates adjacent to the device. Both of these approaches resulted in a costlier design with accompanying tolerance and assembly problems. Filled vias provide a cost effective solution to all of these issues.

By using metals with high thermal conductivity, filled vias provide a heat pipe effect, thermally grounding the junctions of active devices to the package base. From a modeling perspective, the via may be considered as a solid cylinder of metal having thermal conductivity as shown in Table 5. Modern finite element simulation tools also enable the designer to simulate the effects of adding thermal vias. Adding or moving vias may be necessary as a result of a thermal simulation, but the designer should use care to ensure that the previously analyzed electrical performance is not adversely affected.

Assembly concerns with traditional plated holes have centered around the solder and epoxy bleed problems seen during the solder reflow or epoxy curing operations. Filled vias provide an ideal barrier to prevent the introduction of these attachment materials onto the die mounting surfaces. Traditionally, these residue-contaminated areas require a secondary operation to remove excess material, which often results in damage to adjacent circuitry. Not only does this activity add assembly cost, but in the case of solder residue, is usually unsuccessful.

In the rare instances in the past where designers mounted circuits over open vias, care had to be taken in locating via holes relative to bonding pads in order to maintain support under these areas for wire bonding. With Vishay EFI's high planarity filled vias, chip placement with respect to bond pads and vias is now non-critical. This and other important mechanical data is also included in Table 5 to aid the engineer in designing a circuit compatible with modern assembly processes.

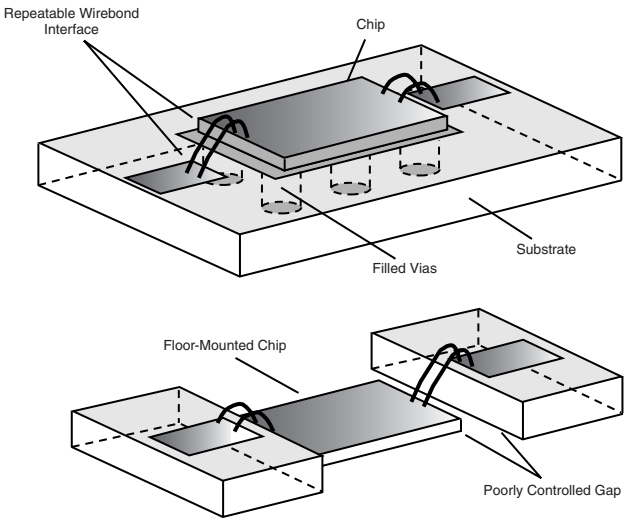

Fig. 4: Device Mounting Approaches, Filled Vias vs Package Floor

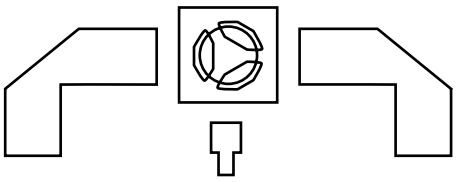

Fig. 5: Vented Via Example

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Table 5 - Plated and Filled Via Thermal and Assembly Data

Parameter	Value	Comment
Thermal Conductivity Gold Copper	300 W/M°C 393 W/M°C	Thermal conductivity of pure Au Thermal conductivity of pure Cu
Filled Via Planarity	+ 0.2/- 0.5 mils (+ 5/- 12.5 µm)	Typical value + 0/- 0.3 mils (Typical value + 0/- 7.5 µm)
Via Location Tolerance	± 2 mils (± 50 µm)	From a fixed datum, Plated or Filled
Via Diameter Tolerance	± 1 mils (± 50 µm)	Plated or Filled, A-Side Surface
Plated Via Capture Pad	Diameter + 0.010" (+ 250 µm)	minimum
Filled Via Capture Pad	Diameter + 0.005" (+ 125 µm)	minimum

Other Applications of Filled Vias

As detailed in other sections of the design guide, filled vias are also used in applications where 2-sided substrates are required. Signals or ground connections may be routed from both sides of the circuit board as shown in Figure 6. Furthermore, Vishay EFI's unique ground-signal-ground technology routes shielded, controlled impedance signal lines using filled vias. For more information, refer to the Ground-Signal-Ground and High Density Digital Interconnect portions of the literature.

Filled Via Hermeticity

All Vishay EFI filled vias exceed MIL-STD-883 method 1014 requirements.

Summary

Filled vias offer circuit engineers a unique opportunity to improve the performance of sensitive designs while providing a more cost effective packaging approach. In addition to reducing the parasitic resistance and inductance of grounding connections, these vias enable thermal management of surface mounted active devices. As an optimal barrier to attachment materials, filled vias reduce assembly costs and reduce piece-part count by eliminating the need for floor mounting active die. For those designs constrained to plated vias, Vishay EFI offers a mature plated via process with flexibility in size and metallization requirements to meet a broad spectrum of circuit applications.

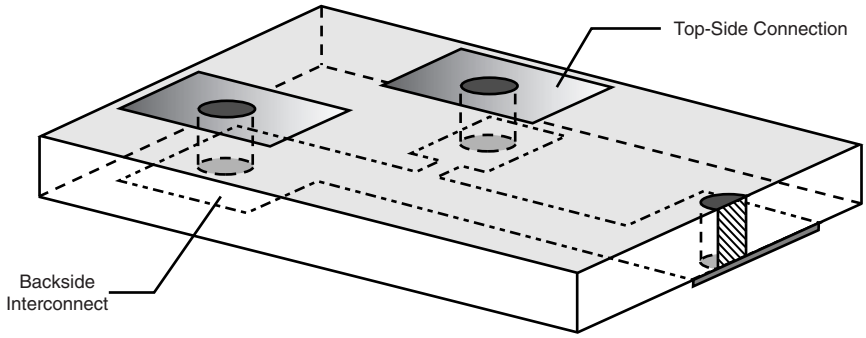

Fig. 6: Two-Sided Signal Routing with Filled Vias

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Additional Tech Notes
Gold or Cu Bumps

In addition to Vishay EFI Au or Cu filled vias, the designer can add Cu or Au Bumps/Posts to the top surface of the substrate for die mounting purposes or to create wire bond pedestils for shortened wire bond lengths. Cu or Au posts can be built up to 5 mil in height as long as the post diameter meets or exceeds the post height (See Fig. 7). Depending on application Cu or Au posts may also be plated with extra Ni + Au layer.

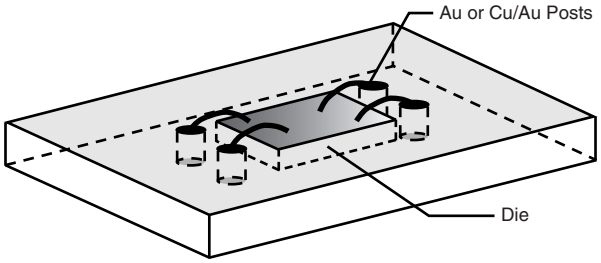

Fig. 7

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